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A Study of Radix-2, Radix-4 and Radix-8 Fast Fourier Transforms using Bidirectional Gate

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ABSTRACT: In the field of Digital Signal Processing, Fast Fourier Transform facilitates signal analysis with the aid of digital computers. It is also one of the fundamental algorithm families in Digital Image Processing and has wide variety of applications in Image Transformation, Sharpening, Smoothing, Edge detection are a few common applications. Fast Fourier Transform is the utilization of algorithms to perform image processing operations on digital images and also rapidly evolving with the emerging applications of Engineering and Science. The broad spectrum applications of Digital Image Processing include remote sensing applications, medical imaging, robotics, acoustic image processing and multimedia transmission. Radix-2, radix-4 and radix-8 decimation in frequency method is designed to execute an efficient FFT architecture. This work mainly focuses on the optimization of FFT architectures for VLSI Implementation. The optimization of FFT designs in this work mainly categorized into two major parts. One is optimization of pipelined FFT designs at the architecture level and the other one is subcomponent minimization. In this paper the study of different types of radix, decimation in time and decimation of frequency fast fourier transform.

KEYWORDS: FFT, Decimation in Time, Decimation in Frequency, real Value data

I. INTRODUCTION

Digital Signal Processing (DSP) is the utmost commanding technology that is shaping Engineering. It has made fanatical changes in a broad range of fields like Health tech, Communication & Telecom, Consumer & portable Electronics, Safety & security, Space, Avionics & Defense to name just a few. Each of these areas has developed a profound DSP technology with owned mathematics, techniques and algorithms. Digital Signal Processing uses digital signals as an input for the processing. It performs mathematical operations to manipulate signals. The main objective of DSP is to measure, compress or filter real world continuous signals. In DSP, Analog to Digital Converter (ADC) applies sampling and digitizing process on to analog signal to convert it to its digital form and then performs mathematical operations on the signal. But to use the signal in real world the signal should be in analog form which again converted using Digital to Analog Converter (DAC). The expeditious development in Very Large Scale Integrated (VLSI) technology has favored the development of faster, miniaturized, less expensive and powerful digital circuits. It has also favored the realization of signal processing operations by means of digital hardware than less reliable analog circuits. All these have led DSP to be in day to day operations like audio recording, video recording, high speed modems and internet access, Image processing, Image compression etc [1, 2]. The signals can be mathematically analyzed both in time domain and equally in frequency domain. The time domain analysis of signals is not suitable for hardware implementation whereas frequency domain analysis provide a better way for real time hardware implementation. Discrete Fourier Transform (DFT) is another imperative tool that represents the frequency domain analysis of a signal. The good nature of Fourier Transform is that it has good energy concentration that leads to extensive scope of applications in Digital Signal Processing and Digital Image Processing. As a result of cumbersome operations and a huge amount of mathematical calculations it has not been widely used [3, 4].

results much faster with lesser 100number of computations. FFTs are fast algorithms i.e., low complexity in the computation of DFT [3]. In an N point DFT computation, the rise in the value of N reflects in the number of complex computations and high computation time. But FFT has reduced the count of computations exceedingly and revolutionized the field of real time processing. The FFT algorithm scales down the sum of complex additions from $N(N-1)$ to $N\log_2N$ and complex multiplications N^2 to $(N/2)\log_2N$. The lesser count of computations is very important criteria in real time

and fast execution in DSP applications. This reduction is possible only because of the decomposition of the total N point DFT into smaller DFTs by availing the periodicity and symmetry property of Twiddle Factor. It is the main component in FFT computation and used uniting the results from the earlier stage to constitute the inputs of the subsequent stage [5].

II. LITERATURE REVIEW

Syeda Farhat Sultana et al. [1], FFT models are planned utilizing the collapsing change and the register minimization strategies. Parallel pipelined structures are determined intricate and genuine esteemed quick Fourier change. The working recurrence of the proposed CFFT design is diminished which diminished the force. Notwithstanding that, the new equal pipelined models RFFT are introduced. The force utilization is decreased up to 37% and half in 2-equal structures separately. Further, the yield tests are gotten in a mixed request.

Navin Nadar et al. [2], have thought about the association of a unique reason processor for on-line. Gold and determined the FFT by progressive information clusters. Notwithstanding portrayal of blended calculations are inferred utilizing the above strategy. The portrayed a basic method to control the FFT equipment. The strategy created the lists both for contributions of each butterfly activity and for the appropriate fidget factor. Notwithstanding that, this technique permits equal association of the memory with the end goal information sources and yields have a place with various memory units, henceforth can generally got to in equal.

Shashidhara. K. S et al. [3], the requirement for fast remote correspondence frameworks has gotten an most extreme need. High information rates lead to extra specialized issues since the broadband radio channel is time variation and show recurrence specific blurring due to multipath proliferation. Along these lines, the channel balance cycle of single transporter frameworks turns out to be excessively confounded. The inspiration to utilize OFDM is to decrease the computational multifaceted nature of high information rate transmission over radio channels. OFDM is a sort of multicarrier transmission, and wherein the radio channel is separated into numerous narrowband subcarriers or sub-channels. The sub-channels are in this manner recurrence non-specific to disentangle the adjustment cycle at the beneficiary. In OFDM framework a solitary information stream is sent over many low rate subcarriers to accomplish equal information transmission. This idea of equal information transmission and FDM was created during the 1960s. In the conventional equal information transmission framework, the absolute recurrence band is partitioned into N non covering sub-channels. Each sub-channel is regulated with a different image, and afterward the N sub-channels are recurrence multiplexed.

Fahad Qureshi et al. [4], have introduced MSR-CORDIC calculation and it's engineering. In MSR-CORDIC calculation miniature turn and scaling tasks are consolidated. The first calculation disposes of target turn point stockpiling. The subsequent calculation. It inferred the advanced arrangement of miniature pivots for the execution of fixed point vector pivot. Further, equipment pre-moving plan is proposed to decrease the barrel shifter unpredictability. These calculations altered the rudimentary pivot conditions. The scale factor is considered as a vital intensity of two. Some cycle was rehashed to expand the ROC. He proposed a scale factor improvement strategy for both exaggerated and roundabout facilitate framework. In this strategy indispensable intensity of two. The scaling activity in the tweet Z change is executed by standardization calculation. The ideal frequencies of CZT are indicated before calculation. Because of this, the aggregate numbers of CORDIC cycles are diminished.

Guilherme Ferreira et al. [5], proposed offbeat exhibit engineering HT. The sans scaling adjusted CORDIC unit is utilized as a fundamental PE. The engineering was reached out to perform round and elliptic HT. In expansion to that these models dispense with the prerequisites of pre-calculations. The point parallelization technique diminished the calculation by 25%. He built up programming characterized. Works in both coordinated and offbeat mode. Clock recurrence chosen the dormancy of the coordinated plan. The CORDIC calculation follows the repetitive parallel number framework and the scale factor is consistent. The calculation proposed in requires both sans scaling CORDIC cycles and ordinary CORDIC cycles and furthermore it builds the circuit unpredictability on account of radix-4 corner encoding. He proposed the CORDIC calculation that totally eliminates the scaling factor.

S. Aseeri et al. [6], depicted bound together exhibit design utilizing changed CORDIC as the fundamental butterfly PE. These four changes are processed by basic re-plan of information tests. Falling the little change engineering can be stretched out to longer length change. Hence these models are appropriate for WSI. In this calculation, the ROC is

improved by area collapsing technique and reparation of some cycle steps. This calculation requires consistent scale factor increase and extra territory for sign/area discovery hardware. Scale factor rectification technique is proposed with one extra clock cycle to play out the estimation contrasted and the ordinary CORDIC calculation. In this calculation, the ROC is expanded utilizing the third-request of Taylor arrangement guess. Calculation in turn mode for exaggerated facilitate. The quantity of microrotation tasks is decreased utilizing the main 1 digit location procedure.

III. FFT ALGORITHM

A quick Fourier change (FFT) is a calculation to process the discrete Fourier change (DFT) and its reverse. Fourier investigation changes over time (or space) to recurrence and the other way around; a FFT quickly registers such changes by factorizing the DFT framework into a result of scanty (for the most part zero) factors. Subsequently, quick Fourier changes are broadly utilized for some applications in building, science, and arithmetic. Demonstrate the butterfly tasks for radix-2 DIF FFT in figure 1 and figure 2. The radix-2 calculations are the most straightforward FFT butterfly calculation.

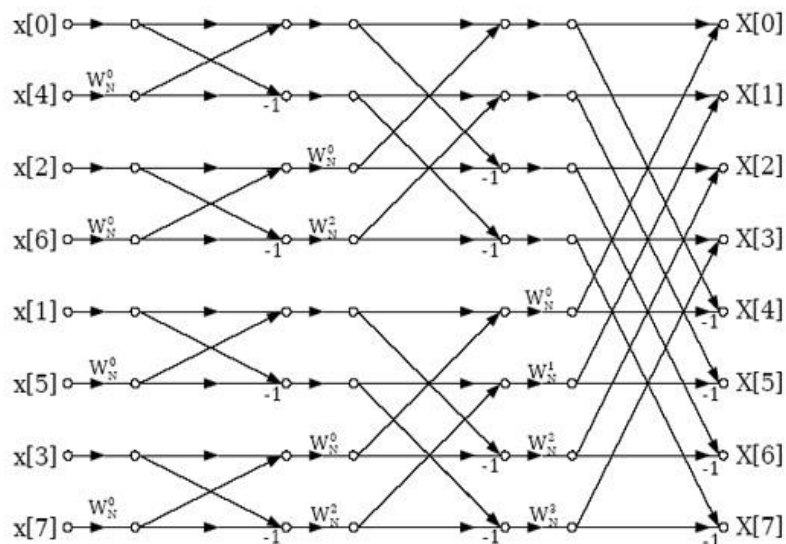


Figure 1: Radix-2 Decimation in Time Domain FFT Algorithm

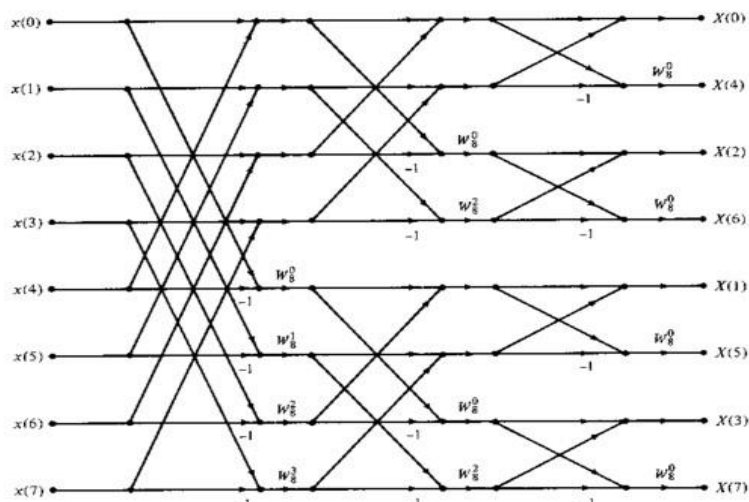


Figure 2: Radix-2 Decimation in Frequency Domain FFT Algorithm

Radix-2

Troublesome to recognize from one another, for this situation the zone based methodology will be calm valuable. Standardized cross connection [13] is a broadly utilized methodology in the territory based technique. Consolidating the stage relationship strategy with methodology was pro acted like an advancement territory based technique interpretation, scale and revolution. Utilized a likelihood thickness inclination based interest direct indicator toward remove the steady point highlights.

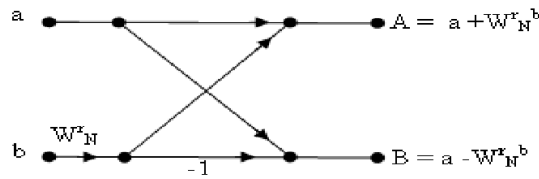


Figure 3: Computation of Butterfly using Radix

They proposed worldwide parallax histogram based channel to dispose of the anomaly actuated by old style connection strategy. He proposed a strategy that utilizes bootstrap resampling to gauge the vulnerability of territory put together picture enlistment calculation with respect to a specific pair of pictures. He proposed a strategy for programmed enlistment. In this, they first applied Harris administrator to remove the corner highlights after that canny administrator is executed to identify the picture edges. The relationship between the picture sets yields the corner focuses. The relative change between the picture pair is set up, which figures the boundaries, as per that the pictures are enlisted.

Radix-3

An iterative calculation to expand picture goal, along with a strategy for picture enlistment with subpixel precision is introduced. He introduced an enlistment strategy that utilizes the Fourier space way to deal with register the objective picture in the source picture. The Fourier technique looks for the ideal match dependent on the data. In view of this unmistakable element it contrasts from other enrollment procedures.

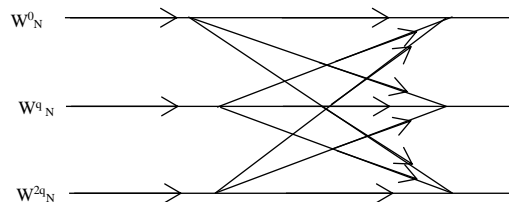


Figure 4: Butterfly element for Radix- 3

They created pseudo-log-polar Fourier change to recognize huge mathematical change. He proposed a versatile polar change rather than log-polar change for enrolling the pictures. They consolidated versatile polar change with projection change alongside coordinating system to recuperate the scale, turn and interpretation.

Radix-4

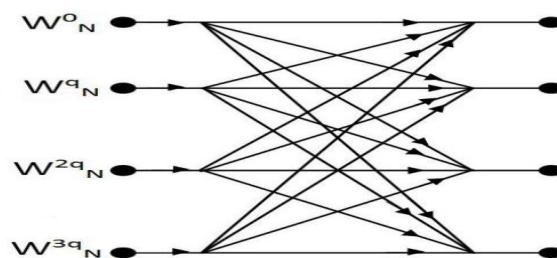


Figure 5: Butterfly element for Radix- 4

Radix-8

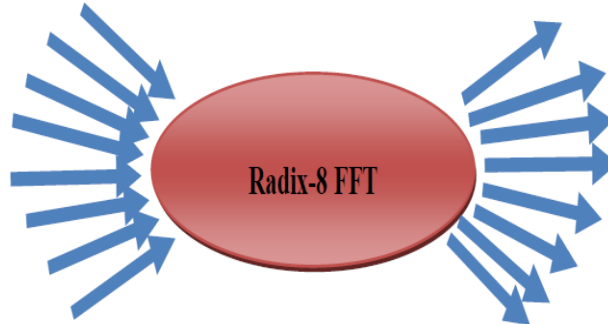


Figure 6: R₈B FFT

IV. BIDIRECTIONAL GATE

Reversible rationale is picking up significance in regions of CMOS configuration in light of its low power dissemination. The conventional entryways like AND, OR, XOR are all irreversible doors. Consider the instance of conventional AND entryway. It comprises of two inputs and one yield. Subsequently, one piece is lost every time a calculation is completed. As indicated by reality table appeared in Fig.1, there are three inputs (1, 0), (0, 1) and (0, 0) that compares to a yield zero. Subsequently it is unrealistic to decide interesting information that brought about the yield zero. With a specific end goal to make an entryway reversible extra info and yield lines are added so that a balanced mapping exists between the information and yield. This keeps the loss of data that is fundamental driver of force scattering in irreversible circuits. The info that is added to an m x n capacity to make it reversible is known as steady information (CI). Every one of the yields of a reversible circuit need not be utilized as a part of the circuit [8]. Those yields that are not utilized as a part of the circuit is called as trash yield (GO). The number of garbage output for a particular reversible gate is not fixed. The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

○ BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 7, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

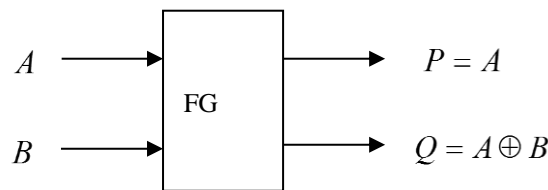


Figure 7: Feynman gate

In figure 8, show the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

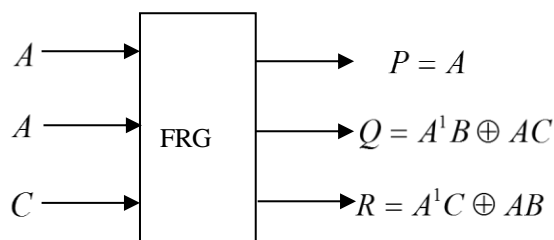


Figure 8: Fredkin gate

Figure 9 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

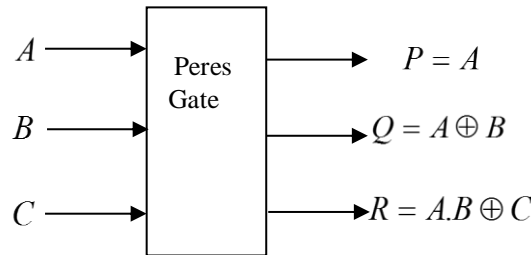


Figure 9: Peres gate

The HNG gate, presented in [10], produces the following logical output calculations:

$$P = A \tag{1}$$

$$Q = B \tag{2}$$

$$R = A \oplus B \oplus C \tag{3}$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \tag{4}$$

The quantum cost and delay of the HNG is 6. At the point when $D = 0$, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 10.

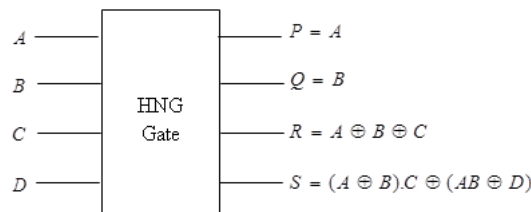


Figure 10: Block Diagram of the HNG Gate

Parameters of Bidirectional (Reversible) Logic

There are many parameters for determining the complexity and performance of circuits in reversible logic circuit design. The following parameters should be reduced for the efficient reversible circuit design [5].

Gate count (N): This refers to the number of reversible gates used in circuit.

Constant inputs (CI): The number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function [5].

Garbage outputs (GO): The number of unused outputs present in a reversible logic circuit. Garbage outputs can't be avoided as these are essential to achieve reversibility.

Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate.

Gate levels (GL): The number of levels in the circuit which are required to realize the given logic functions [5].

V. CONCLUSION

Many research works on the Design of FFT and IFFT architectures have been reported in recent years. Still there is a much room for the improvement of the architecture to improve Speed and the memory requirement. In this thesis, as an initial step the FFT and IFFT of color images was obtained to study the effects different architectures. During the study it was realized a need to design a time efficient VLSI architectures for FFT and its Inverse to overcome the large computational time involved in the intensive calculations of FFT. So the designing of VLSI architectures for FFT and its Inverse was started. During the design it was also realized a problem in storing the huge amount of image data in terms of megabytes.

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